Transforming Concepts To Reality: New Technologies for New Applications

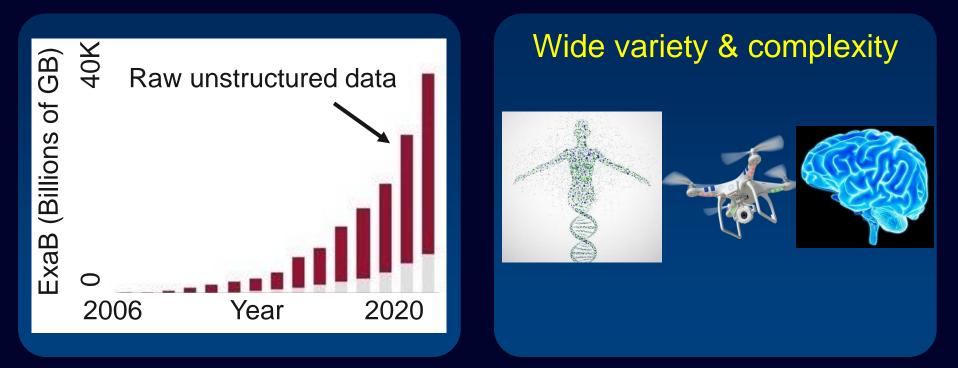
Max M. Shulaker



Massachusetts Institute of Technology

Data Explosion

"Swimming in sensors, drowning in data"



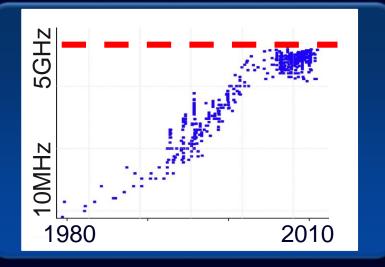
Mine, search, analyze data in real-time

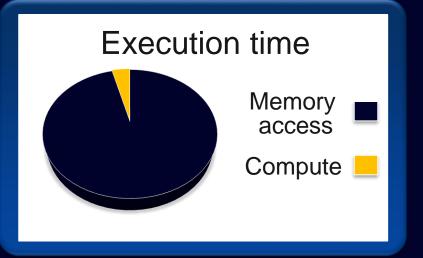
Data centers, mobile phones, robots

Many Obstacles <u>Simultaneously</u>

Power Wall

Memory Wall





Communication Wall

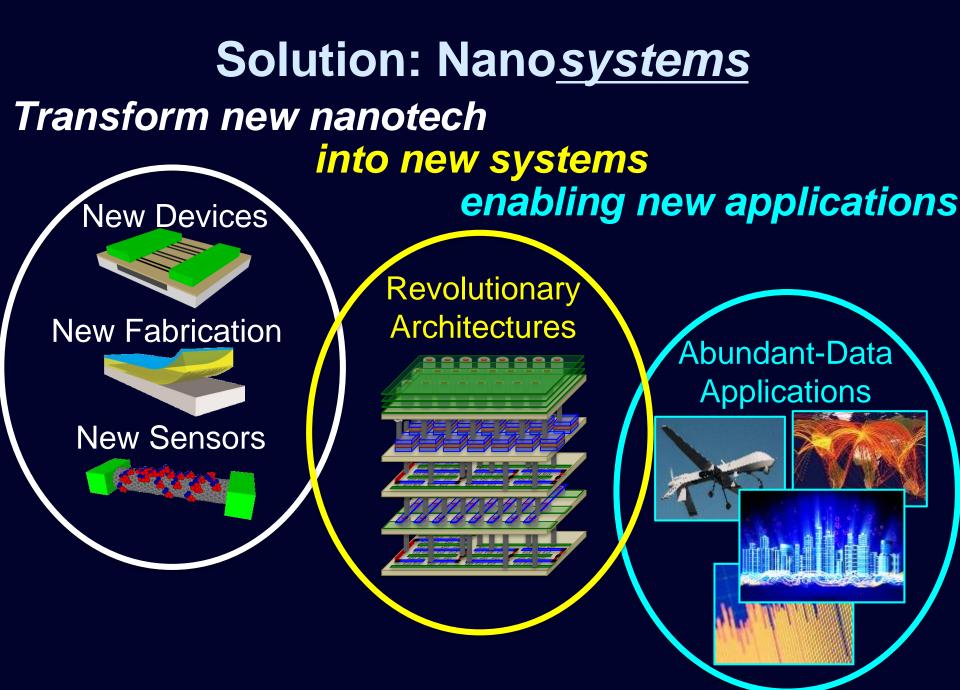


Also: interconnect wall, complexity wall, resilience wall...

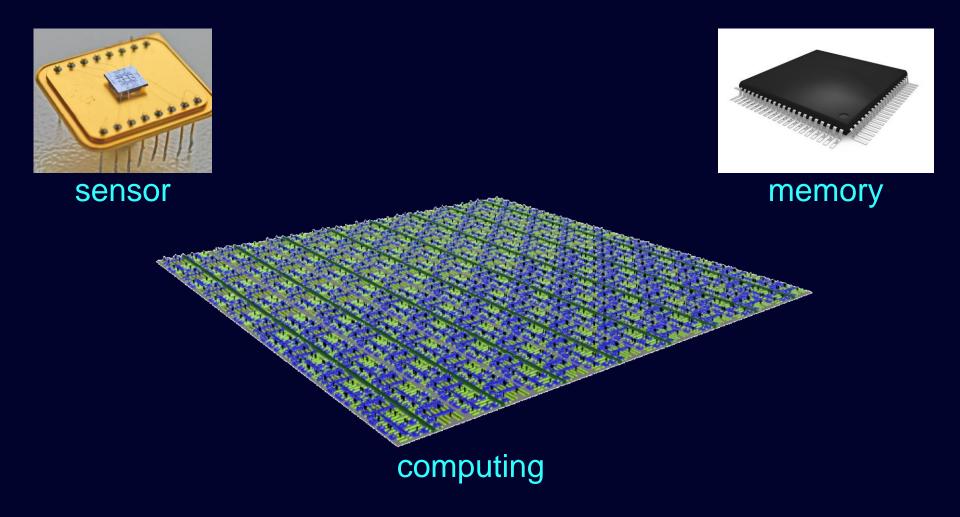
Enabling New Applications:

Nanosystems

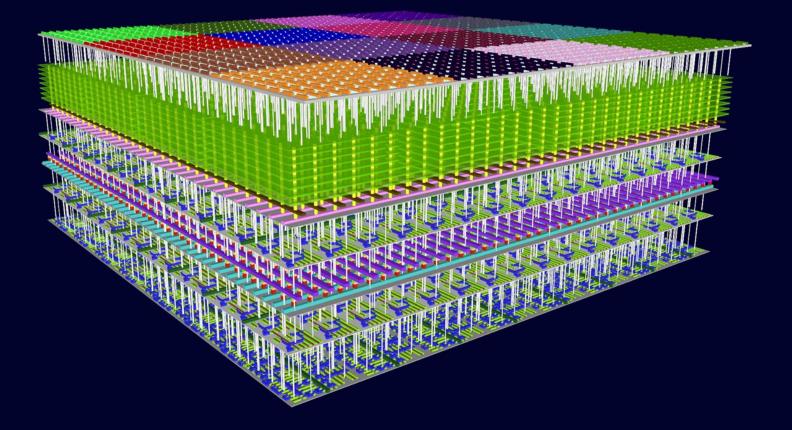
new sensors better transistors novel memories new architectures thermal management improved algorithms yield and reliability



Systems Today 2-Dimensional

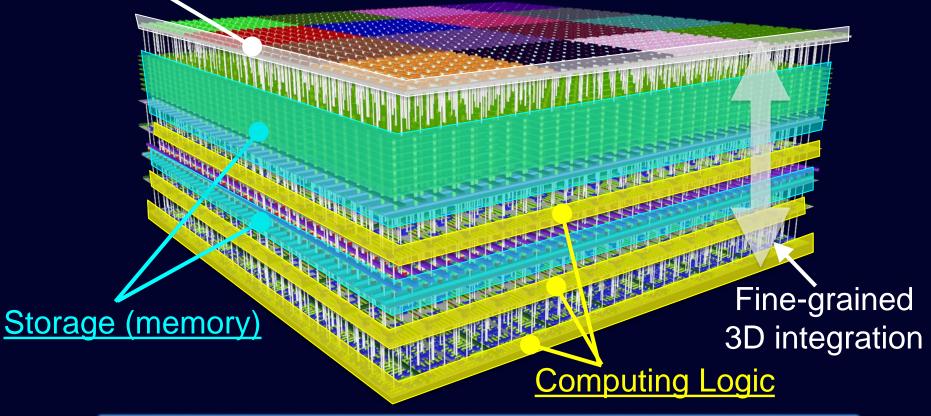


Future Nanosystems



Future Nanosystems

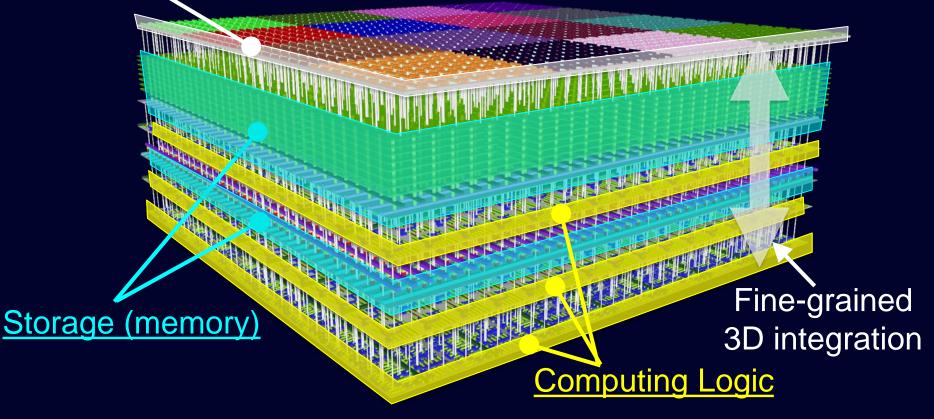
Increased Functionality



Impossible with today's technologies

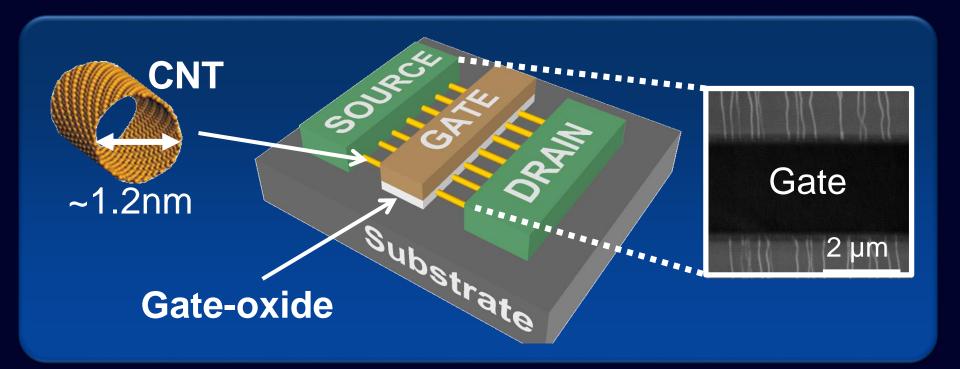
Realizing Nanosystems TODAY Enabled by Emerging Nanotechnologies

Increased Functionality

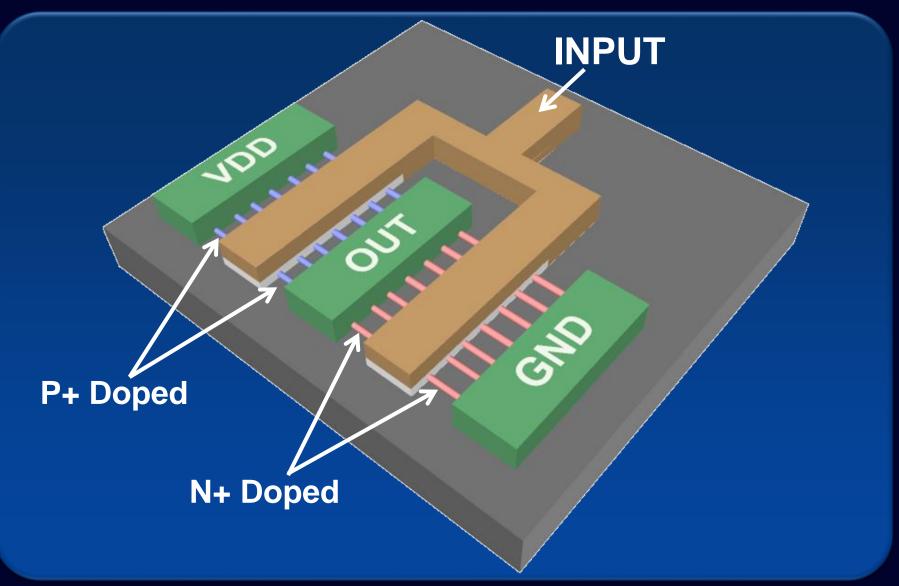


Carbon Nanotube FET (CNFET)

- Energy efficiency: ~10X benefit ^[1]
- Chemical sensors: ideal candidate



Ideal CNFET Inverter



Ideal CNFET sensor

INPUT

Functionalization

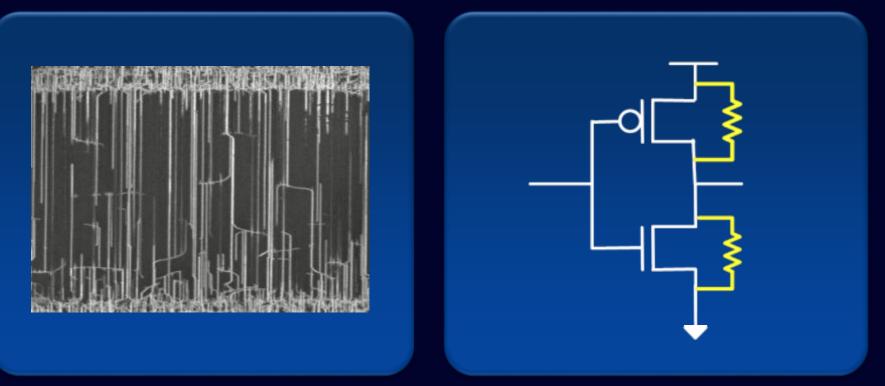
(metal porphyrin, DNA, SAMs, polymers, etc.)

JDE

BIG Promise, BUT Major Obstacles

Mis-positioned CNTs

Metallic CNTs



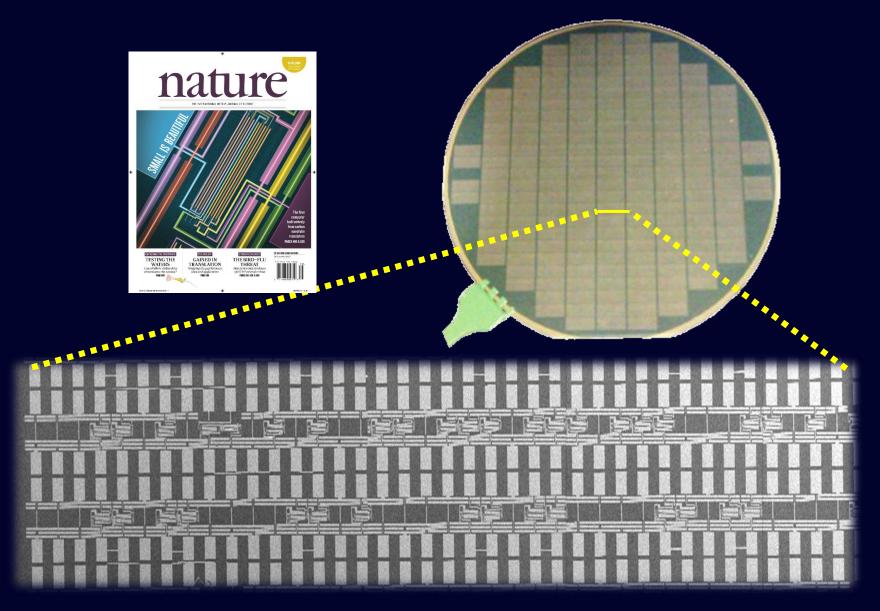
Combined processing + design solutions

Most Importantly

- VLSI processing
 - No per-unit customization

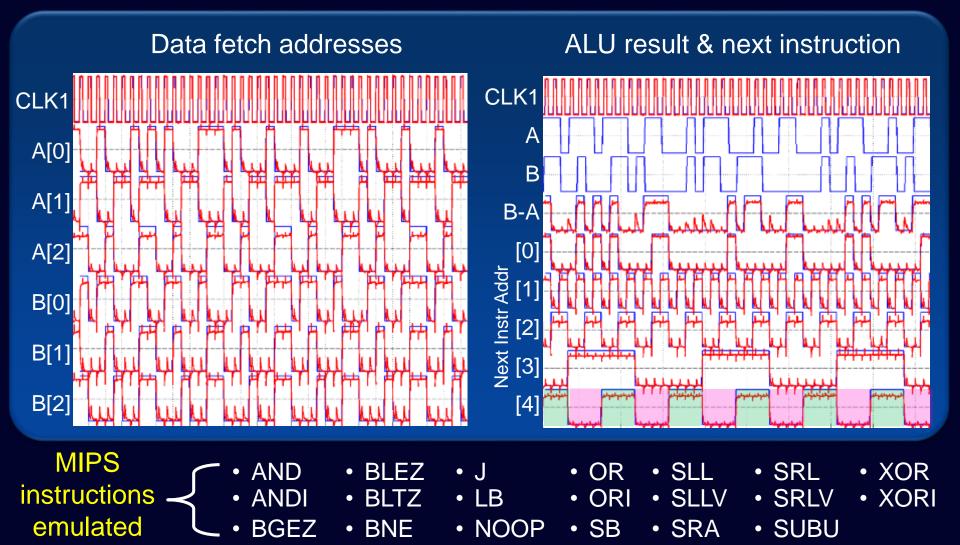
- VLSI design flow
 - Immune CNT library

CNT Computer

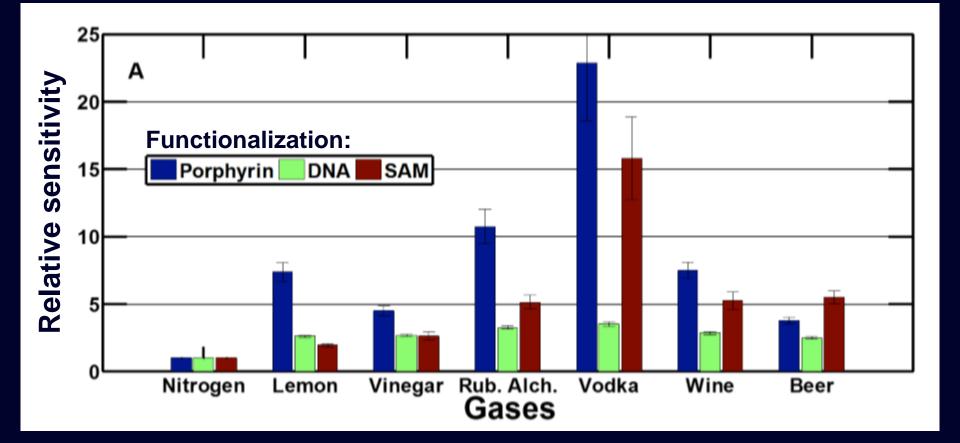


[Shulaker Nature 13] Collaborators: G. Hills, N. Patil, H. Wei, H. Chen, H.-S.P. Wong, S. Mitra

Multi-Tasking Concurrent programs: Sort, Count



CNFET Gas Sensors



How do we do better?

3D Integration

Massive ILV density > TSV density

Through silicon via (TSV)

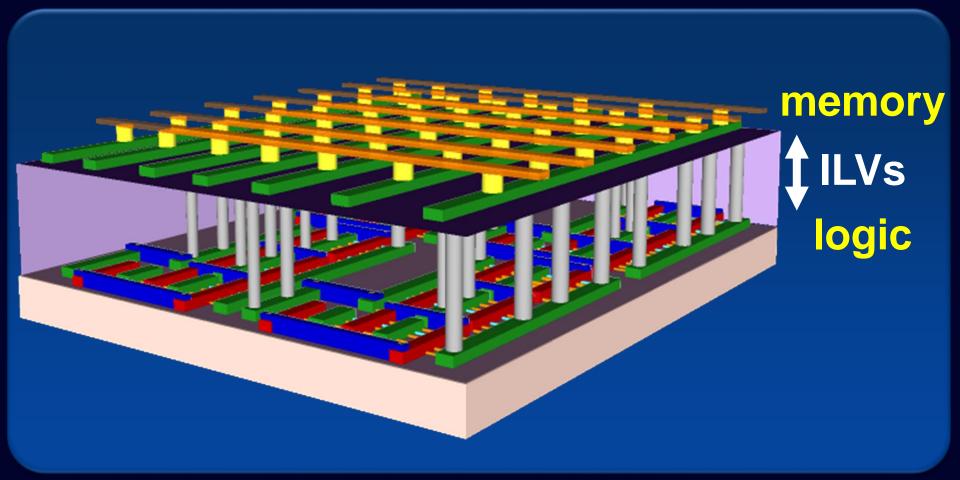
TSV (chip stacking)

Monolithic

Nano-scale inter-layer vias (ILVs)

Monolithic 3D: Logic + Memory + Sensing

Increased data bandwidth



Energy and Performance Benefits

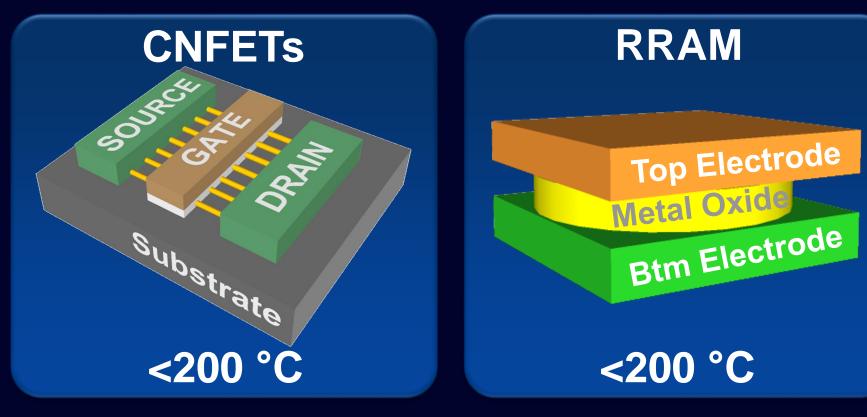
- Memory access time
 - Less processor idle time
- Memory access energy
 - Memory + logic stacking
- Resource Contention
 - Wide connectivity

Realizing Monolithic 3D

- Low-temperature fabrication: <400 °C
 - Major obstacle for silicon CMOS

Realizing Monolithic 3D

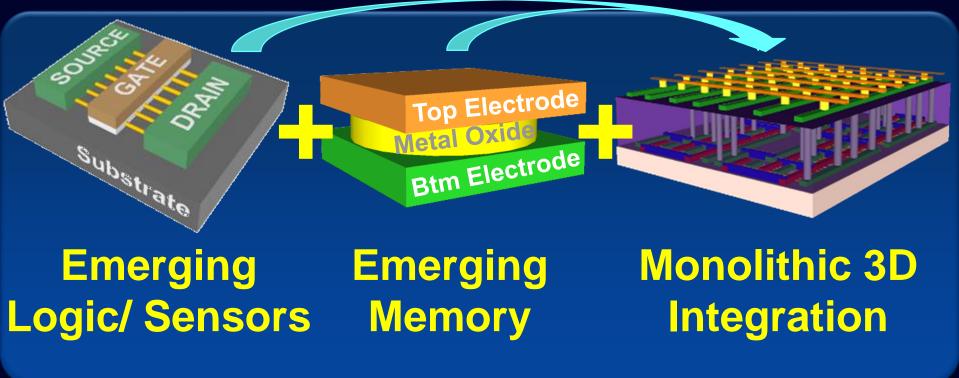
Low-temperature fabrication: <400 °C
Logic/ Sensing Memory

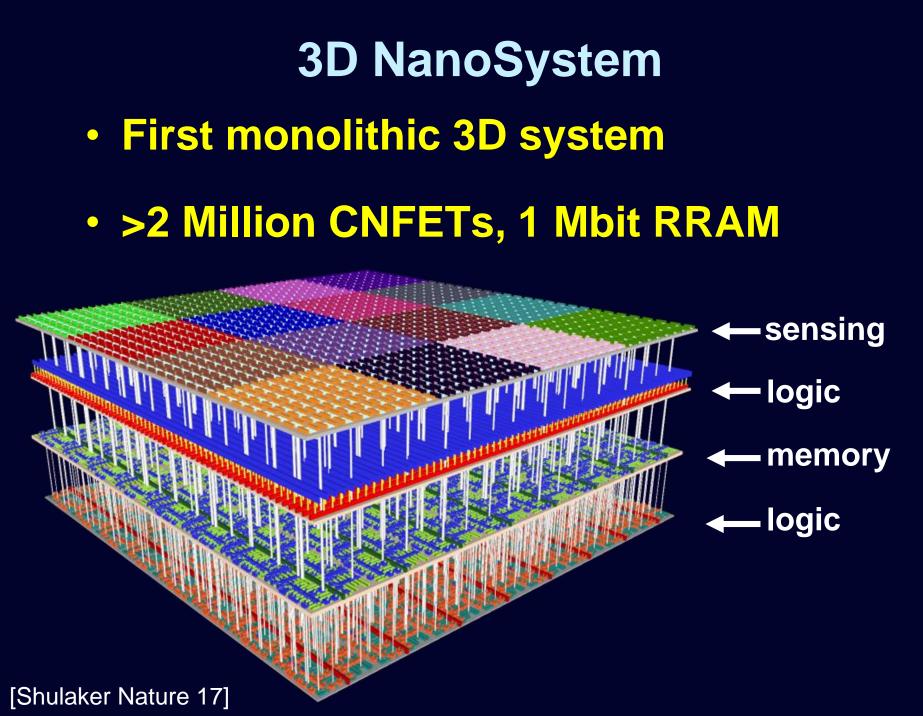


Realizing Monolithic 3D

Combine device + architectural benefits

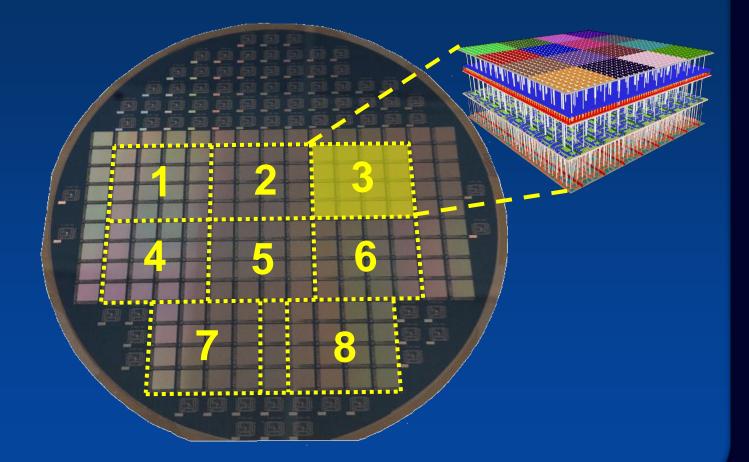
Naturally enabled





NOT Just a Cartoon

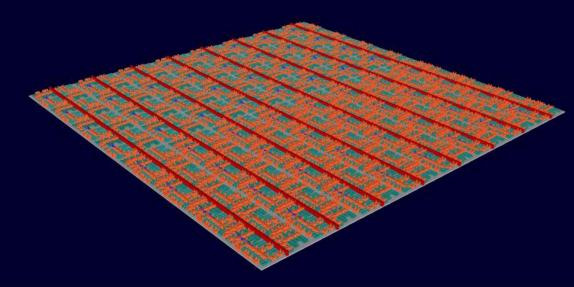
Wafer-scale design + fabrication



• Starting substrate

Silicon FETs

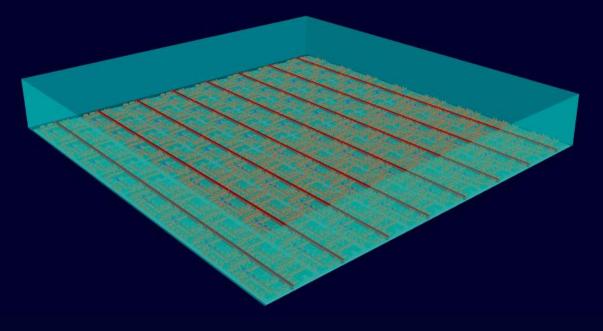
1050 °C dopant activation



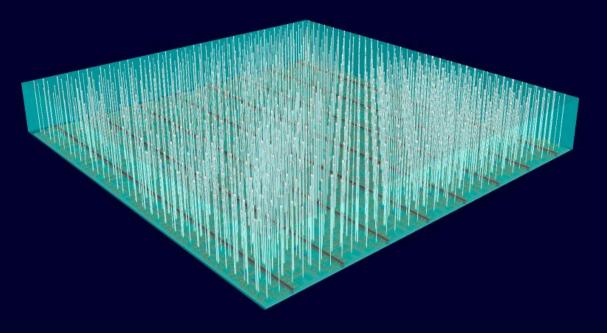
1. Bottom layer only

2. Silicon OR CNFET

• Inter-layer dielectric (ILD)

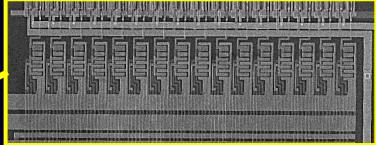


- Inter-layer vias (ILVs)
 - Ultra-dense vertical inter-connects

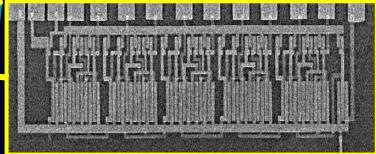


CNFET logic

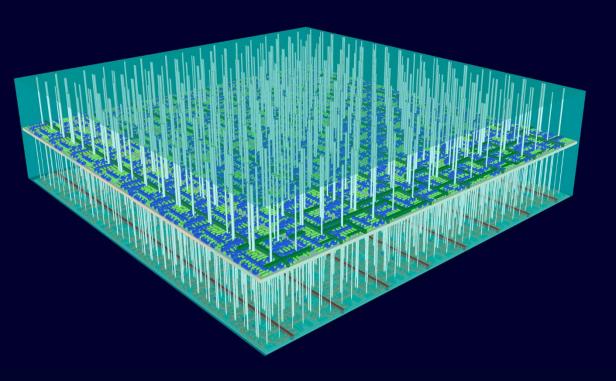
Memory access circuitry



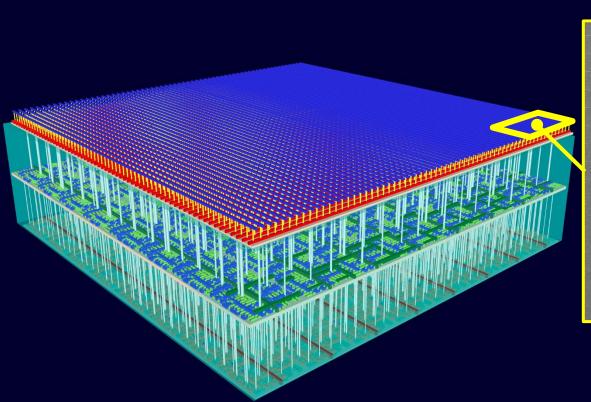
Classification accelerator on-chip computation



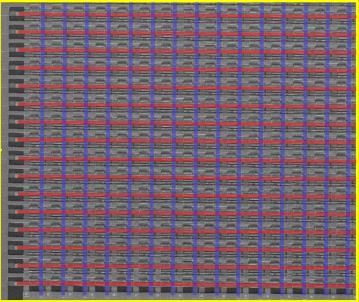
• 2nd ILD + ILVs



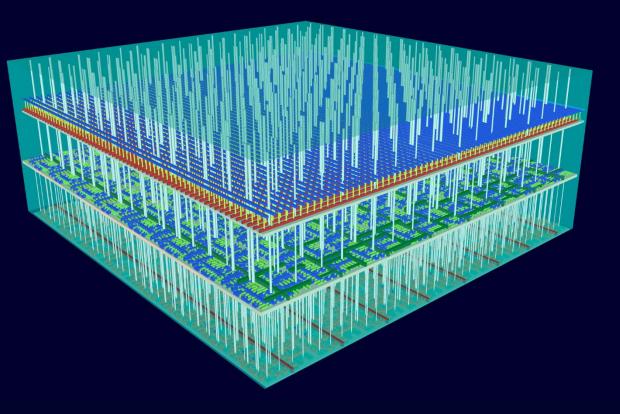
Memory: RRAM



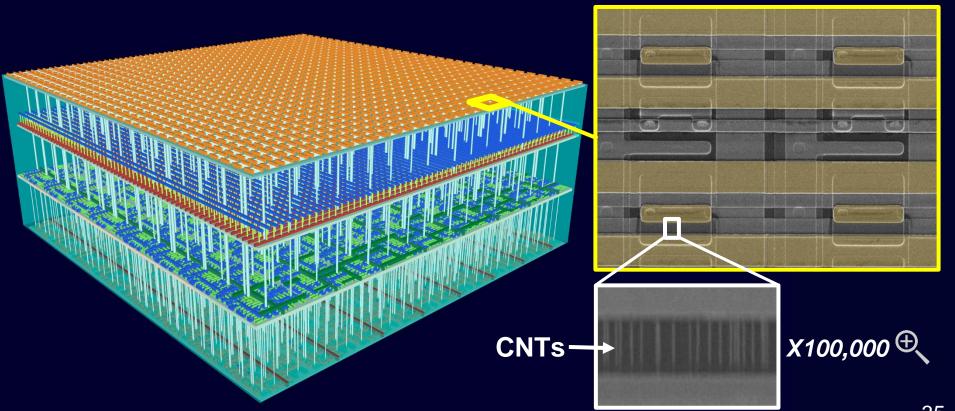
RRAM array: 1 Mbit



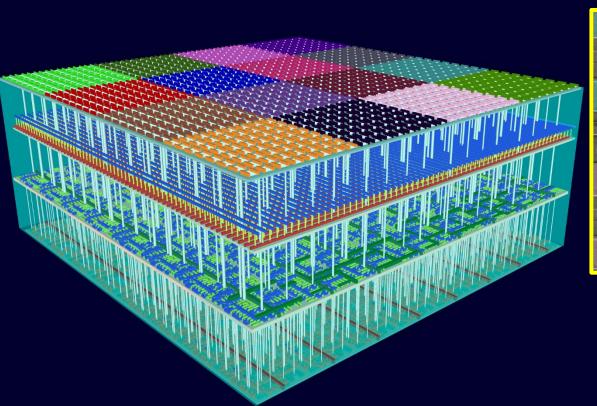
• 3rd ILD + ILVs



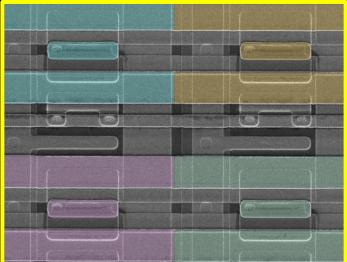
• CNFET logic

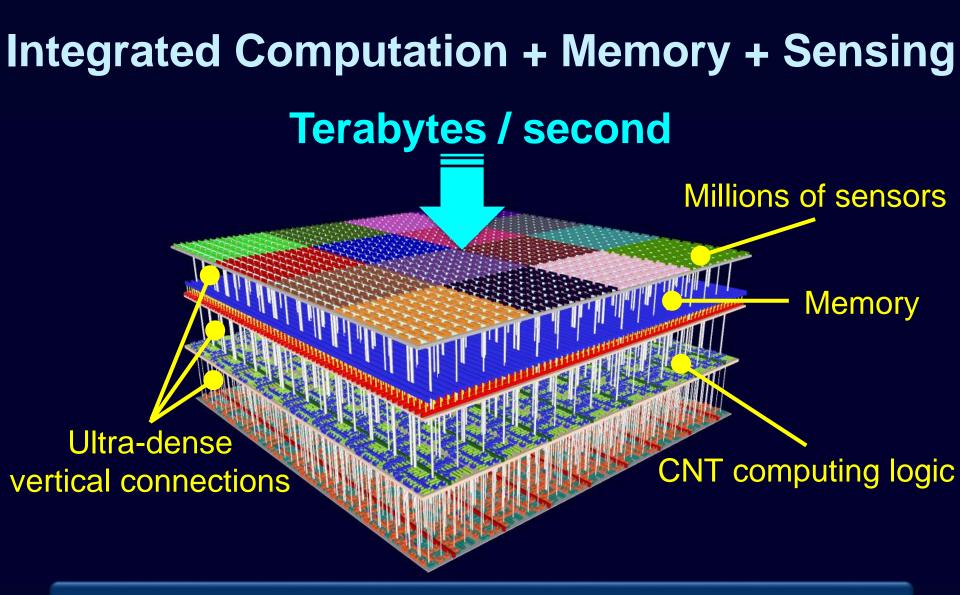


CNFET functionalization



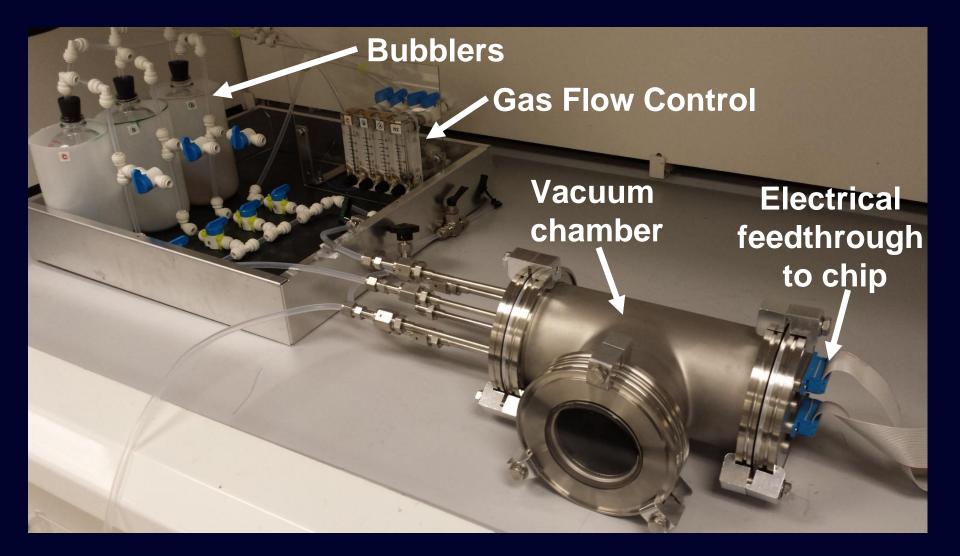
>1 million gas sensors





Abundant sensor data: Extensive + accurate classification

Experimental Demo

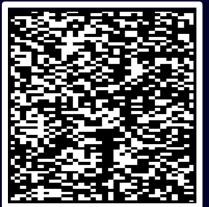


Raw Data

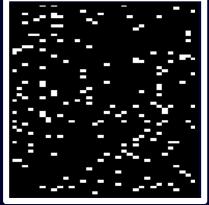
Sensor data written to RRAM array

CNFET classification accelerator

Lemon Juice



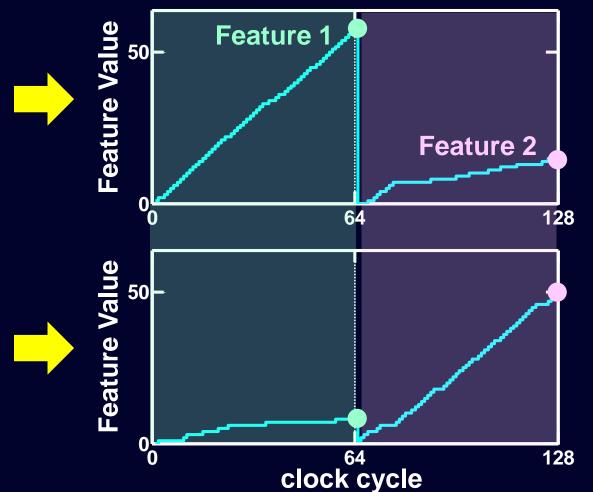
Rubbing Alcohol



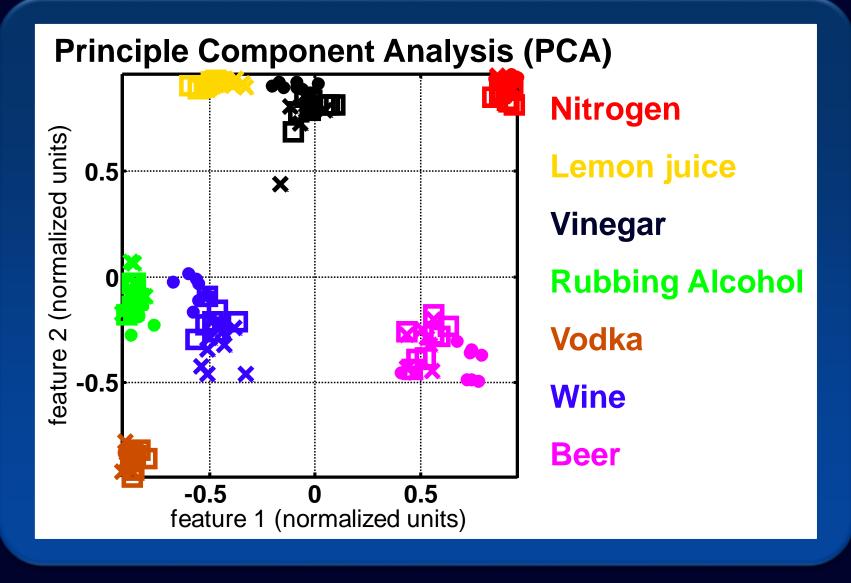
[Shulaker Nature 17]

Measured Output

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Experimental Results

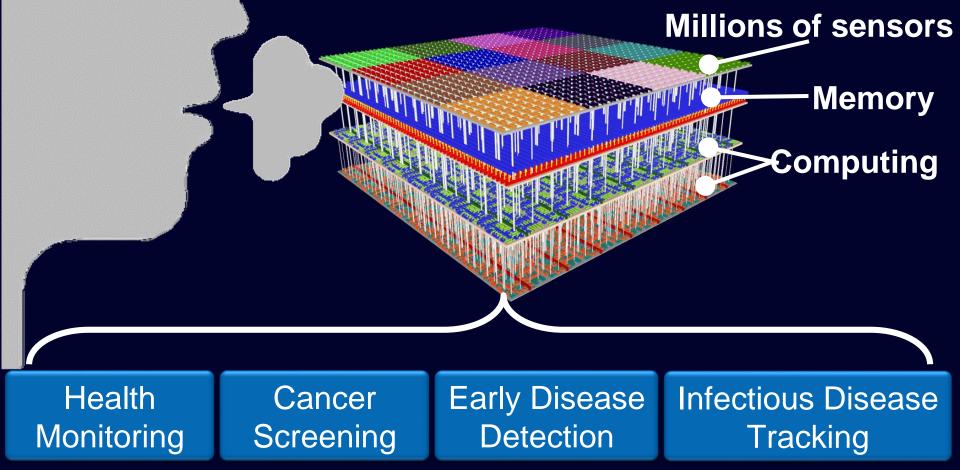


- Energy-efficient logic + memory
 - Heterogeneous integration

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 - Heterogeneous integration
- High bandwidth communication
 - Fine-grained 3D integration

- Energy-efficient logic + memory
 - Heterogeneous integration
- High bandwidth communication
 - Fine-grained 3D integration
- Transform massive data into useful info
 - Sensing immersed in computation + memory





New Technologies -> New Applications



Conclusion

- Nanosystems useful today
 - Exciting opportunities
- New solutions: elegantly simple
 - <u>Combined</u> processing + circuit design

