

MIT Industrial Liaison Program Faculty Knowledgebase Report

Shaping the Future of Semiconductors

April 23, 2026 10:00 am - 11:00 am

10:00AM

Welcome and Introduction
Hong Fan
Program Director, [MIT Industrial Liaison Program](#)



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Hong Fan is a Program Director at the Office of Corporate Relations at MIT. She joined OCR in August 2016, brought with her 20+ years of international work experience across semiconductor, consumer electronics, telecom, and higher education.

Prior to joining OCR, Hong spent 12 years in the semiconductor industry with executive functions in strategic marketing, business development, corporate strategy, product management, and product marketing at Analog Devices and MediaTek. During those years, Hong played instrumental roles in identifying emerging business opportunities related to wireless communication networks, smartphones, wearable devices, Internet of Things (IoT), and medical devices and applications. She led cross-functional teams in defining and driving product and market strategy for businesses with annual revenue ranging from \$30 million to \$100 million.

Prior to joining the semiconductor industry, Hong spent 6 years in the telecommunications and electronics industry, leading engineering teams at companies such as Lucent Technologies and Watkins-Johnson Company for the development of digital signal processing, wireless communications, and micro-controller software.

Before coming to US, Hong was a strategic research staff at the President Office of Shanghai Jiao Tong University, one of the oldest universities in China. She was the first woman to hold this highly selective position.

Hong has a B.S in Electronic Engineering from Shanghai Jiao Tong University, an M.S. in Electrical Engineering from University of Maryland at College Park, and an MBA from Sloan School of Management at MIT. She received numerous academic honors and awards including the McKinsey & Co. Scholarship, the NSF Graduate Research Fellowship, and the Shanghai Outstanding College Graduate Award.

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AI-Powered Data Centers: Building a Sustainable Future by Scaling the Package
Anuradha Agarwal

Principal Research Scientist,
[MIT Microphotonics Center/ Materials Processing Center](#)



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Dr. Anuradha Agarwal is a Principal Research Scientist at [MIT's Microphotonics Center and Materials Research Laboratory](#).

Her research includes the integration of active and passive optical components on silicon, using standard Si-CMOS fabrication processes. Her work on MIR linear and nonlinear materials and devices is creating a planar, integrated, Si-CMOS-compatible microphotonics platform, which is enabling on-chip imaging and sensing applications.

As the leader of the LEAP or Lab for Education and Application Prototypes at MIT.nano, she (i) builds a roadmap document of photonic sensors through the Integrated Photonic Systems Roadmap – International (IPSR-I), by identifying technology gaps in materials, components and systems for photonic sensors, and (ii) enables education and workforce development in integrated photonics across the human talent pipeline from K to Gray.

As director of the Electronic-Photonic Packaging (EPP) program at MIT's Microphotonics Center, she is exploring innovative photonic testing and packaging solutions towards resource efficiency across technology, value chain innovation, and workforce in the supply chain.

Anuradha was named a 2022 Optica Fellow with over 250 refereed publications, 21 awarded patents, and 1 pending patent. Prior to coming to MIT, she received her doctoral degree in Electrical Engineering from Boston University, where she investigated the spatial extent of point defect interactions in silicon. With Dr. Agarwal's cross-disciplinary training in Physics, Electrical Engineering, and Materials Science, and industrial experience, she has successfully connected basic sciences with relevant applications, using integrated devices that are manufacturable on a large scale.

Energy consumption is at an all-time high in data centers. Enhanced microchip functionality for next-generation applications, such as AI, 6G, LiDAR etc., can no longer depend solely on shrinking the dimensions of a transistor. **The semiconductor package including electronic-photonic integration is the 21st-century transistor, and this must be scaled to obtain high-performance systems.**

Generative-AI (Gen-AI) models require massive and rapid data movement between thousands of interconnected processors (GPUs/XPUs) and memory systems. Traditional electrical interconnects, which rely on long traces on a circuit board and power-hungry pluggable optical modules, have reached their physical and energy limits. The electrical signals degrade over distance, requiring additional components like digital signal processors (DSPs) and retimers, which consume significant power and add latency.

Co-packaged optics (CPO) is essential for this recent Gen-AI-driven revolution because it directly addresses the critical bottlenecks of power consumption, bandwidth density, and latency that are crippling traditional data center architectures. CPO overcomes these limitations by integrating optical engines directly onto the same package as the processing chip (ASIC). This dramatically shortens the electrical path from centimeters to mere millimeters, allowing data to be converted to light and transmitted much more efficiently.

Through FUTUR-IC, a global research alliance, we are enabling a transformative industry-driven solution that simultaneously optimizes across three critical dimensions of system Technology, Value chain innovation, and Workforce development, to ensure commercial viability across the semiconductor supply chain. Our CPO innovations within microchip systems, offer high-performance, passively assembled chip-to-chip and chip-to-fiber couplers which employ graded-index, evanescent, and reflector structures, and are fabricated using standard complementary metal-oxide-semiconductor foundry processes.

The urgency to align microchip system performance scaling with a commercially viable manufacturing value chain dominates business and technology decisions today, as the solutions are expected to power the next 40 years of progress for the semiconductor industry.

10:30AM

High-Power Terahertz Generation On-Chip

Ruonan Han

[MIT Electrical Engineering & Computer Science \(EECS\)](#)

10:58AM

Closing

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