MIT Industrial Liaison Program Faculty Knowledgebase Report

After Moore's Law (Repeat)

October 21, 2020 7:30 pm - 9:50 pm

All timings below based on Eastern Standard Time Zone.

7:30pm

Welcome and Introduction
Jewan Bae
Director, MIT Corporate Relations/Industrial Liaison Program

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Jewan John Bae comes to MIT Corporate Relations with more than 20 years of experience in the specialty chemicals and construction industries. He facilitates fruitful relationships between MIT and the industry, engaging with executive level managers to understand their business challenges and match them with resources within the MIT innovation ecosystem to help meet their business objectives.

Bae’s areas of expertise include new product commercialization stage gate process, portfolio management & resource planning, and strategic planning. He has held various business leadership positions at W.R. Grace & Co., the manufacturer of high-performance specialty chemicals and materials, including Director of Strategic Planning & Process, Director of Sales in the Americas, and Global Strategic Marketing Director. Bae is a recipient of the US Army Commendation Medal in 1986.

7:35pm

MIT's Interdisciplinary Materials Research Laboratory
Carl V. Thompson
Director, Materials Research Laboratory (MRL)

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Professor Thompson joined the MIT faculty in 1983. He is Director of MIT's Materials Research Laboratory and co-Director of the Skoltech Center for Electrochemical Energy Storage. His research interests include processing of thin films and nanostructures for applications in microelectronic, microelectromechanical, and electrochemical systems. Current activities focus on development of thin film batteries for autonomous microsystems, IC interconnect and GaN-based device reliability, and morphological stability of thin films and nano-scale structures. Thompson holds an SB in materials science and engineering from MIT and a PhD in applied physics from Harvard University.

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(Carl Thompson video time stamps starts at 3:25)

7:55pm

Keeping Silicon Great: Silicon IC's Incorporating New Devices
Eugene A. Fitzgerald
Merton C. Flemings SMA Professor of Materials Science and Engineering, MIT Department of Materials Science and Engineering

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Merton C. Flemings SMA Professor of Materials Science and Engineering
MIT Department of Materials Science and Engineering

Eugene A. Fitzgerald is the Merton C. Flemings SMA Professor of Materials Engineering at the Massachusetts Institute of Technology. Building upon his early experience at AT&T Bell Labs which included the invention of high mobility strained silicon, he has created fundamental innovations in stages from early technology to final implementation in the market. His research interests include novel thin film materials and devices. He is the founder, co-founder, or founding team member of AmberWave Systems Corporation, Contour Semiconductor, 4Power LLC (high-efficiency III-V solar on silicon), Paradigm Research LLC, and The Water Initiative. He is co-author of "Inside Real Innovation", published internationally in January 2011. He is the recipient of the IEEE 2011 Andrew S. Grove Award, the IEEE 2004 EDS George Smith Award, and the TMS 1994 Robert Lansing Hardy Medal Award. He received a BS degree in Materials Science and Engineering in 1985 from MIT and his Ph.D. in the same discipline from Cornell University in 1989.

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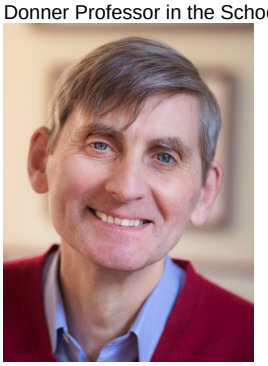
Mankind's insatiable desire for connectivity, communication, computation, and improvement in standards of living will continue to drive transitions in integrated circuit technology, as it has done in the past. As increasing transistor density no longer delivers the required value, new directions will appear to build the future integrated circuits that continue to drive these holistic needs. Designing silicon integrated circuits enabled by inserting new devices is such a path of new value. III-V devices have been monolithically integrated into silicon manufacturing processes, demonstrating novel functionality in silicon circuits containing GaN LEDs and GaN transistors. The methods used for monolithic incorporation of III-V devices into silicon ICs are independent of a particular material or device, so such methods could continue to keep silicon great far into the future.

8:25pm

3D integration: above and beyond Moore's Law
Jesús A. del Alamo
Donner Professor in the School of Engineering



Jesús A. del Alamo
Donner Professor in the School of Engineering

Jesus A. del Alamo is the Donner Professor and Professor of Electrical Engineering at Massachusetts Institute of Technology. He obtained a Telecommunications Engineer degree from the Polytechnic University of Madrid and MS and PhD degrees in Electrical Engineering from Stanford University. From 1985 to 1988 he was with Nippon Telegraph and Telephone LSI Laboratories in Japan and since 1988 he has been with the Department of Electrical Engineering and Computer Science of Massachusetts Institute of Technology. From 2013 until 2019, he served as Director of the Microsystems Technology Laboratories at MIT. His current research interests are focused on nanoelectronics based on compound semiconductors and ultra-wide bandgap semiconductors.

Prof. del Alamo was an NSF Presidential Young Investigator. He is a member of the Royal Spanish Academy of Engineering and Fellow of the Institute of Electrical and Electronics Engineers, the American Physical Society and the Materials Research Society. He is the recipient of the Intel Outstanding Researcher Award in Emerging Research Devices, the Semiconductor Research Corporation Technical Excellence Award, the IEEE Electron Devices Society Education Award, the University Researcher Award by Semiconductor Industry Association and Semiconductor Research Corporation, the IPRM Award and the IEEE Cledo Brunetti Award. He currently serves as Editor-in-Chief of IEEE Electron Device Letters. He is the author of "Integrated Microelectronic Devices: Physics and Modeling" (Pearson 2017, 880 pages), a rigorous and up to date description of transistors and other contemporary microelectronic devices.

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Much has been written about "The End of Moore's Law" for over a decade. The term evokes a picture of stalled computing performance. Reality is far from this doomsday scenario and the outlook of information processing technology appears brighter than ever. Certainly, as transistor footprint scaling is quickly approaching a regime in which "smaller is no longer better," a radical redirection is mandatory. The new path is the third dimension, piling transistors on top of each other in a 3D construction. The promise goes beyond the integration of more transistors per unit area to keep the economic incentives behind Moore's Law. The third dimension opens new possibilities to bring together logic and memory and break the "memory wall", the current bottleneck for system performance. Intimate memory and logic integration will also enable artificial intelligence chips capable of efficiently processing very large data sets. This talk will outline opportunities and challenges for future IC technologies while showcasing relevant MIT research on new materials (i.e. magnetics, interconnects,), devices (i.e. carbon nanotubes transistors, tunnel transistors, neuromorphic devices), process technology (monolithic 3D integration), etc.

8:55pm

Invited Presentation Lightning Talks – Invited MIT Students and Postdocs

Topics covered:

- CNT microprocessors
- Graphene-enabled remote epitaxy
- Ferroelectric materials for steep-subthreshold CMOS
- CNT-based 3D systems: integrated sensors and imagers
- Neuromorphic proton-based devices
- Li-based neuromorphic materials and devices
- Growth of 2D materials for electronics
- Integrated thin-film batteries
- 2D electronic materials and devices
- Quantum computing technology, different aspects
- 3D IC thermal management

As part of the program for this webinar, we are offering breakout discussions with our presenting graduate students and postdocs. **In order to participate in these breakout rooms, you will need the latest version of Zoom (version 5.3.2)**. (If you need help determining your version of Zoom, please follow the instructions here.)

If you do not already have this version, **please update your Zoom client/application before joining the discussion**. Follow the instructions here to update Zoom.

9:15pm Parallel Lightning Presentation Break-out Discussions

Room #	Topic / Invited Presenter / Position	Title and Abstract	Supervisor
Room 1	2D electronic materials and devices Ahmad Zubair Post Doc	**Two-dimensional Materials: The Future of Hetergeneous Integration** Layered two-dimensional materials offer unique advantages for heterogeneous integration thanks to their atomically thin body, van der Waals nature of interlayer bonding, relatively low growth temperature and wide range of electronic, optical and mechanical properties. These properties allow seamless back-end-of-the-line integration of novel devices, circuits and systems on a Si CMOS platform to develop complex 3D systems. This combination can not only push the performance limits of existing technologies but also enable new functionalities which current CMOS technologies cannot offer.	Prof. Tomas Palacios
Room 2	CNT-based 3D systems: integrated sensors and imagers Tathagata Srimani Grad Student	**Heterogeneous Integration of BEOL Logic and Memory in a Commercial Foundry: Carbon Nanotube Logic and Resistive RAM** Monolithic three-dimensional (3D) integration enables revolutionary digital system architectures with vertically-interleaving layers of logic and memories, with dense and fine-grained connectivity. Such monolithic 3D systems promise significant (>100x) energy-efficiency improvements over conventional two-dimensional systems. Here we show BEOL integration of multi-tier carbon nanotube field-effect transistor logic and Resistive RAM within a commercial foundry at a 130 nm technology node. We also fabricate and experimentally validate a wide range of digital systems (3D imager, RISC-V microprocessor etc). All design and fabrication is VLSI-compatible and leverages existing silicon CMOS infrastructure.	Prof. Max Shulaker
Room 3	CNT microprocessors Christian Lau Grad Student	**Modern Microprocessor Built from Complementary Carbon Nanotube Transistors** Electronics is approaching a major paradigm shift because silicon transistor scaling no longer yields historical energy-efficiency benefits, spurring research towards beyond-silicon nanotechnologies. In particular, carbon nanotube field-effect transistor (CNFET)-based digital circuits promise substantial energy-efficiency benefits, but the inability to perfectly control nanoscale defects and variability in carbon nanotubes has precluded the realization of very-large-scale integrated systems. Here we overcome these challenges to demonstrate a beyond-silicon microprocessor built entirely from CNFETs. The microprocessor runs standard 32-bit RISC-V instructions on 16-bit data and addresses, comprises more than 14,000 complementary CNFETs and is designed and fabricated using industry-standard design flows and processes	Prof. Max Shulaker

9:50pm	Wrap-up