Germanium: Low Cost, High Performance Solar Cells and Novel Photonics Devices

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Outline

- Motivation
- Ge-on-Si Integration
- Threading Dislocation Reduction in Ge
- Ge Lateral Overgrowth
- Ge Photodetectors for BEOL Integration
- Conclusions
Dispersive Micro-concentrator Solar Cell Concept

- Hi-dispersion micro-prism array spectrally disperses DNI sunlight
- Low-dispersive micro-prism array cancels beam deviation but maintains dispersion
- Concentrating optics focuses light onto lateral multi-junction cells
- Secondary optic consists of a hollow reflective DNI concentrator and a solid diffuse concentrator
- Molded primary and secondary optical element arrays
- Compact micro-CPV: module thickness < 2.5cm

MIT PIs: J. Michel, J.J. Hu, E.A. Fitzgerald, D. Perrault
Epitaxial Laterally Arrayed III-V Solar Cells

- Low-cost, high quality heteroepitaxy Ge-on-Si film
- Selective growth and lateral overgrowth to achieve below $10^6$ cm$^{-2}$ threading dislocation density
- High efficiency InGaP cells on Ge demonstrated
Threading Dislocation Reduction and Solar Cell $V_{oc}$

- Defect trap states from dislocations in GaAs and InGaP solar cells

**GaAs**


**InGaP**

Kim et al. submitted

Target TDD $< 10^6 \text{ cm}^{-2}$
Separate absorption and charge multiplication APD.

Quantum Si Photonics, Paul Davids, Sandia 2016
Dark Count Measurement

Two Dark Current mechanisms:
1) Thermal Generation
2) Tunneling
Both in Si and Ge.
Measured Dark Counts

Position within gate window is stochastic.

Dark count triggers Geiger response.
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Ge Epitaxy on Si

Fig. 7.12. Illustration of two crystals with mismatched lattice constant resulting in dislocations at or near the interface between the two semiconductors.

Ge epitaxial growth on Si at 550C
Limited TDD Reduction by Dislocation Reactions

Create thermal stress between Si/Ge to induce dislocation glide

10⁹ cm⁻²

10⁷ cm⁻²

Limitation to TDD reduction in blanket, thin Ge films


G. Wang, APL 94, 102115 (2009)
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Limited TDD reduction in selectively-grown Ge

- Further dislocation reduction by introducing dislocation sinks
  - Selective chemical vapor deposition of Ge on Si between SiO$_2$ sidewalls
  - Threading dislocations leave film at edges
  - TDD in mesa center reduced to $2 \times 10^6$ cm$^{-2}$ for 10 µm x 10 µm mesas

- Limitation to TDD removal by dislocation sinks
- Can Ge lateral overgrowth lead to low TDD Ge films?


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Ge Lateral Overgrowth: Can it work?


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Lateral Overgrowth between Ge Strips

High Ge/SiO$_2$ surface energy: Reduced growth rates, voids

Once coalescence is complete, further growth self-planarizes

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Delayed ELO from Ge Mesa Corners

- Film growth at mesa convex corners becomes bounded by slow growing facets

Complete film coalescence over mesa corners is severely delayed
Increased Coalescence Rates in Staggered Grids

- Eliminate coalescence points entirely dependent on growth from convex mesa corners

Time required before complete coalescence reduced by > 50%

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Accelerated ELO above Isolated Sidewall Lines

- Remove all convex corners
- Guarantee film edges for all threading dislocation to reach

Complete film coalescence occurs more readily due to concave Ge film perimeter

On-axis coalesced film

Off-axis coalesced film

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Increased Coalescence Rate for Narrow Isolated Lines

Overgrowth at zero and negative concavity Ge film perimeters

Accelerated coalescence increases for reduced line widths

1.0 µm wide isolated SiO$_2$ lines

0.5 µm wide isolated SiO$_2$ lines
Optimal Sidewall Line Misorientation for Coalescence

ELO maximized for line orientations between $0^\circ$ and $15^\circ$ away from the intersection of $\{111\}$ planes with the substrate surface.

Optimal offset $5^\circ$ to $\{111\}$ surface intersection directions.
Threading dislocation densities reduction for Ge-on-Si substrates

Patterned Ge: \( \sim 10^6 \text{ cm}^{-2} \)

Optical microscope for Ge-on-Si, patterned and unpatterned Ge show significant difference in threading dislocation densities.

TDD can be reduced to below \( 10^6 \text{ cm}^{-2} \) in small areas. Lateral overgrowth should extend low TDD across entire wafer.

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Electronic-Photonic ‘CMOS’

Photonic Integration Scenarios

Bulk Si
Si FET

SOI
Photonic Integration Scenarios

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BEOL Single Crystal Ge Devices

- Confine growth vertically AND laterally on amorphous Si
- Limit process temperature to 450°C

K.A. McComber, J.F. Liu, X. Duan, J. Michel, L.C. Kimerling, 
Back-End MSM Photodetectors

- Structural damage from pre-metallization clean
- BEOL compatible Ge responds reacts differently to clean than epi-Ge

Chemical cleaning damages BEOL compatible Ge
Ge Photodetectors: Comparison with Literature

- State of the art detectors on crystalline Ge
- First device to demonstrate QE > 100%
- MSM on amorphous substrates exhibit potential, but need to decrease leakage current

First device to demonstrate QE > 100%
Conclusions

- Low TDD Ge-on-Si has the potential to enable novel devices and low cost substrates for III-V materials and devices.
- Ge-on-Si based III-V solar cells will reduce cost by at least 10x.
- Ge single photon detectors for room temperature operation in the near IR are possible.
- High performance Ge BEOL photodetectors are viable for low temperature processing.
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